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Identification Of Property Of Ultra High Frequency Carrier Wave Based Tera/Zetta Hertz PRBS Generator- $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 For Advanced Digital Satellite Wireless Communication

Prof. Executive Dean. P.N.V.M Sastry[1], Prof. Dr. Srinivasan Vathsal [2]
Former Industry Principal Engineer DV(USA)
(Former VG Of Synopsys, Intel, FPT Software ,CYIENT MFG EDS) & Past Executive Dean & Prof IT EDA Software MNC Industry And R&D)
[1](VLSI Department, Silicon Interfaces, India)
[2](ER&IPR Cell, Retd., Director, DRDO HQ, India)

Abstract:
Recent years Application Design verification and RTL Engineers and scientists facing biggest challenge on effective quality moderate long distance high speed high frequency wireless communication system designs to get original high quality modulated and demodulated serial/ parallel signal with effective frequency bandwidth spectrum and baud rate data transfer without signal loss/ distortion, signal interference noise and degradation, timing violations, glitches, crosstalk, frequency notes, Bandwidth spectrum etc. Due to we proposed new Identification of property of Ultra high frequency carrier wave based Tera/Zetta Hertz PRBS tapped pattern Generators – $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for Advanced digital satellite wireless communication systems. The PRBS Carrier Generator ASIC for Ultra High Speed Long Distance Communication Hi-tech Smart Computing Products like Cloud & Internet Computing, LTE ASIC, WiFi, GiFi, OFDMA WCDMA, QCDMA, GPS satellite Technologies etc. Basically The design contains Tera/ zetta hertz clock frequency synchronized PRBS Generators of Different Tapped Sequences existing are $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 etc as well proposed one's are $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 etc and Multiplexer. These different pattern sequences are Designated as per CCITT ITU Standards. Design compilation, simulation and synthesis done by leading eda software design tools (Synopsys 2021.1v) as well Design flow Implemented by Xilinx ISE 9.2i IDE Software and RTL Design verification done by System Verilog HDL/ Verilog HDL
***Background**: The proposed PRBS generators generates ultra high frequency carrier waves of different tapped sequence seed word data stream patterns $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for long distance digital satellite multi user system application (CDMA, GPS et..) to protect low frequency base band signal for long distance multiple lacks of kilometers. Why we have choosen long periodicity PRBS of different length 48,51,63,127,255 to generate efficient effective high quality carrier waves as well for modulation and demodulation of Transmitter and Receiver at Tera/ Zetta hertz clock frequency. All these PRBS generators are designed using Linear Feedback shift registers of different length.*
***Materials and Methods**: In this prospective the design and verification of PRBS generators done by RTL design block architecture and HDL Verilog/ system Verilog design method/ approach. Logic synthesis done by Xilinx The design compilation and simulation verification done by leading eda software design tools Synopsys vcs 2021.1. Logic fpga synthesis done by Xilinx ISE 9.2i IDE.*
***Results**: RTL Design and verification done for PRBS Generators of different tapped seed word patterns 48,51,63,127,255. Verified simulation and synthesis results. Analyzed display results and wave forms of ultra high frequency carrier waves.*
***Conclusion:** RTL Design and verification of Tera/Zetta Hertz PRBS tapped pattern Generator – $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for Advanced digital satellite wireless communication systems.*
***Keyword**: PRBS Pseudo random binary sequence, CCITT- consulting committee for international telegraph and telephone, ITU- International Telecom unit, RTL- Register transfer level, HDL- Hardware description language, ASIC- Application specific integrated circuit, GPS- Global position system.*

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I. Introduction

In the modern digital wireless satellite communication systems speed and long distance communication is a major constraint factor for advanced digital satellite application system designs. Due to we proposed new Tera/ Zetta hertz Speed (tbps/ zbps baud rate) high frequency PRBS carrier generator ASIC of different

seed word pattern length 48,51,63,127,255. I design tera bits per second/ zetta bits per second high speed PRBS Pseudo random binary sequence carrier frequency generators generate ultra high random frequency carrier wave data in the form of different deterministic random frequency numbers of different speed and frequency w.r.t specific data tapping sequence elements/ seeds. The multichannel PRBS generators designed for generation of ultra high frequency carrier waves for long distance satellite user applications to reception of data is in the RANDOM Sense, This PRBS generators designed for Identification property of Different Tapped PRBS Sequences 48,51,63,127,255 etc at a clock frequency speed of Tera Hertz THz and Zetta Hertz ZHz and the Length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. This is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, Wireless OFDMA , CDMA,QCDMA, WiFi Computing, wireless internet computing, cloud computing etc because of data transfer speed baud rate in terms Tera bits per second (Tbps)/ Zetta bits per second(Zbps). These are newly proposed tapping elements based PRBS generator designs *$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1. Earlier designs are* according to ITU O.150, O.151, and O.152 standards up to 31 tapped elements. This PRBS Design consists of multiplexer, PRBS Registers of different tapped sequence points, clock Frequency Generators of Tera Hertz / Zetta Hertz Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & CRC

II. Material And Methods

[A] Tera Hertz Clock Generator

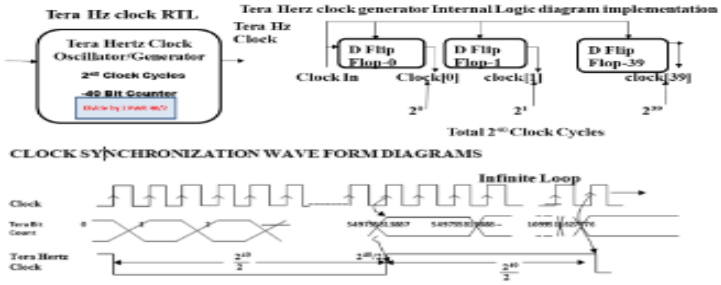


Figure 1. Tera Hertz Clock generator- RTL, Internal logic diagram & clock synchronization wave form

[1] Tera Hertz clock generator consists of 40 bit counter generate 2^{40} Clock cycles of 1 complete Tera hertz clock cycle.

[2] Tera Hertz clock output of one full clock cycle generated at the 2^{40} th count value by increment the count value of 549,755,813,888.

[3] If we make count = count+40'b1000_0000_00……; on the very next clock period tera hertz clock generated due to this we reduced number of clock cycles period for improvement of high speed and performance, access latency.

[4] The Tera Hertz Clock pulse low and high toggling happens at every 2 power 40 divided by 2 clock = 549,755,813,888 count value.

[5] The tera hertz positive clock edge/negative clock edge trigger happens at every 549,755,813,888 count value.

[B] Zetta Hertz Clock Generator

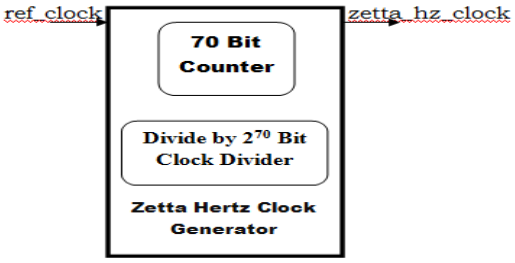


Figure 2. Zetta Hertz Clock generator

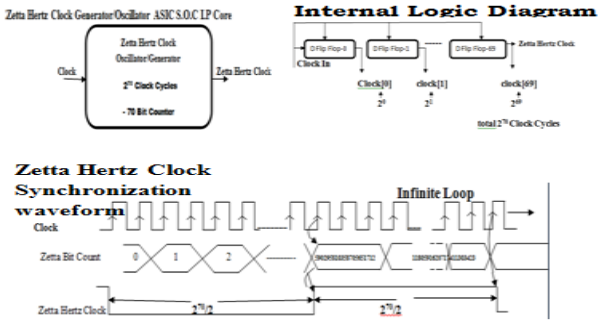


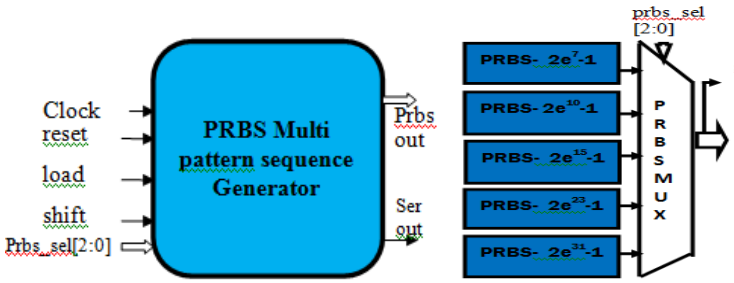
Figure 3. Zetta Hertz clock synchronization wave form

Description: The Above Figure 8.10 Zetta hertz Clock generator, It consists of Divide by 2^{70} Clock Divider we can easily generate baud rate frequency with these Clock Dividers. It consists of 70 bit counter, one input as reference clock (500KHz) and output as Zetta Hz clock generated at every $2^{70}/2$ count of 500KHz reference clock cycles Zetta hertz clock toggled mean i.e.,Every $2^{70}/2$ count of 500KHz reference clock cycles time takes Zetta hertz clock high period and subsequent $2^{70}/2$ count of 500KHz reference clock cycles time takes Zetta hertz clock low period done by increment of count value of every $2^{70}/2$ Clock Cycles reference and also reduction of number clocks totally reduced and looks like normal reference clock after doing simulation.

- Zetta Hertz clock generator consists of 70 bit counter generate 2^{70} Clock cycles of 1 complete Zetta hertz clock cycle.
- Zetta Hertz clock output of one full clock cycle generated at the 2^{70}th count value by increment the count value of 5.90295810E+20.
- if we make count = count+70'b1000_0000_0000_0000_00….; on the very next clock period Zetta hertz clock generated due to this we reduced number of clock cycles period for improvement of high speed and performance, access latency.
- The Zetta Hertz Clock pulse low and high toggling happens at every 2 power 70 divided by 2 clock = 5.90295810E+20 count value.
- The Zetta hertz positive clock edge/negative clock edge trigger happens at every count value of 5.90295810E+20.

[2] PRBS Design Architectures

[A] Existing RTL Design Architecture and Logic design Of PRBS Generator for Identification of property of various patterns of seed word Tapped sequences [$2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1]



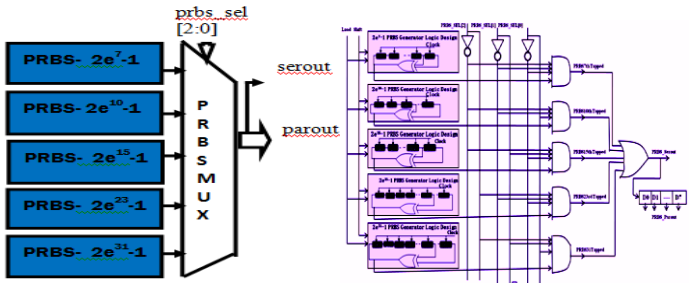


Figure 4: RTL Design Architecture Figure 5: Logic design of PRBS generator

PRBS Generators for Identification of property of various patterns $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1.

Description: The above diagram shown Multi channel PRBS Generator generates one of the PRBS $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 Tapped sequence pattern through channel 8:1 multiplexing. The channel multiplexing done through PRBS selector lines[2:0]. The multi channel PRBS Consists of 8:1 Multiplexer, different PRBS Pattern Generators -(2^7-1,2^{10}-1, 2^{15}-1,2^{23}-1,2^{31}-1 etc. The multiplexer chooses one of the many PRBS Pattern Sequences, feeds it to the D-FF Register, and sends it in either parallel or serial output mode. The Above figure(1) shows RTL Design Architecture for PRBS multi pattern sequence generator for Identification of property of various seed patterns $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 word Tapped sequences. It consists clock, reset, load and shift and PRBS-sel[2:0] as inputs and PRBS parallel and serial outputs.The $2e^7$-1 PRBS Generator includes 8-bit LFSR. The LFSR contains 8 D type Flip flops with feedback tapped DFF element positions(7,6) and the tapped positions 7 and 6 are XORED (compared) bit by bit and generates output. The output is feed back as input to the 8- bit LFSR. Similarly Other PRBS generators of various data bit lengths of (10, 16, 24, 32 Dtype Flip Flops) with feed back tapping position DFF elements (10,3),(14,15),(18,23),(28,31) are xored and generates serial and parallel output of specified PRBS "$2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1".The purpose of tapping the elements of PRBS is for generate standard specific high frequency and baud rate under CCITT & ITU standards.The PRBS generates 256 random seed word numbers repeatedly. Based on the concept of n bit PRBS, The PRBS Generator contains n number of D type Flip flopelements. The Maximum length of PRBS is 2^L-1. The above figure(2) shows Logic Design Architecture for PRBS Generators of identification of property of various PRBS Patterns – "$2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1". This PRBS generator includes 8:1 multiplexer and 3 PRBS select lines The PRBS selector select particular PRBS pattern of above mentioned and generates PRBS output in the form of serial and parallel output.PRBS sequences are produced with LFSR with different set of tapping polynomials under C.C.I.T.T – I.T.U Telecom Standards. Some common sequence generating polynomials are PRBS 7 = $1 + x^6 + x^7$ PRBS 10 = $1 + x^3 + x^{10}$ PRBS 15 = $1 + x^{14} + x^{15}$ PRBS 23 = $1 + x^{18} + x^{23}$

[B] Proposed RTL Design Architecture OF PRBS Generator for Identification of property of various patterns of seed word Tapped sequences [$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1].

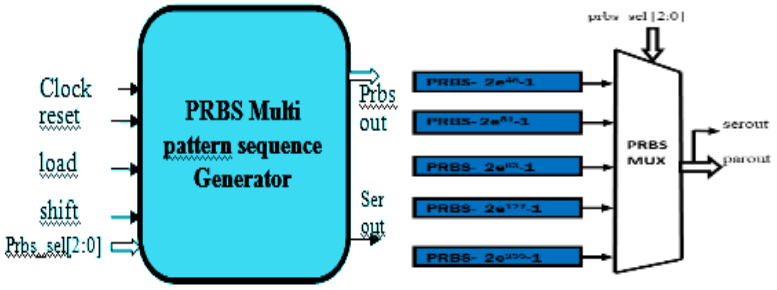


Figure 7: Proposed RTL Design Architecture and Logic Design for PRBS Generators for Identification of property of various patterns $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1

The above figure shows Logic Design Architecture for PRBS Generators of identification of property of various PRBS Patterns – "$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1". The PRBS generator includes 8:1 multiplexer and 3 PRBS select lines The PRBS selector select particular PRBS pattern of above mentioned and generates PRBS output in the form of serial and parallel output.

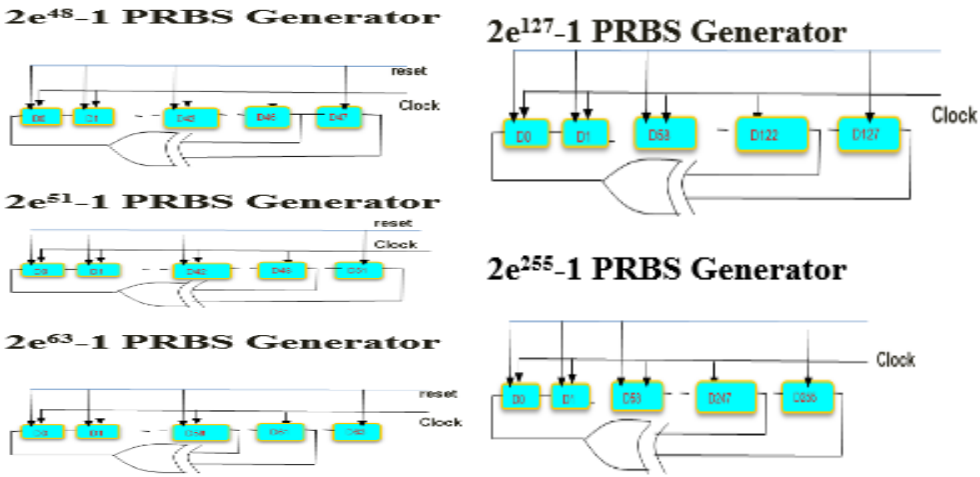


Figure 8: PRBS Generators for Identification of property of various patterns $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1

[A1] Proposed Ultra High Frequency (Mega, Giga, Tera, Peta, Exa, Zetta Hz PRBS Model

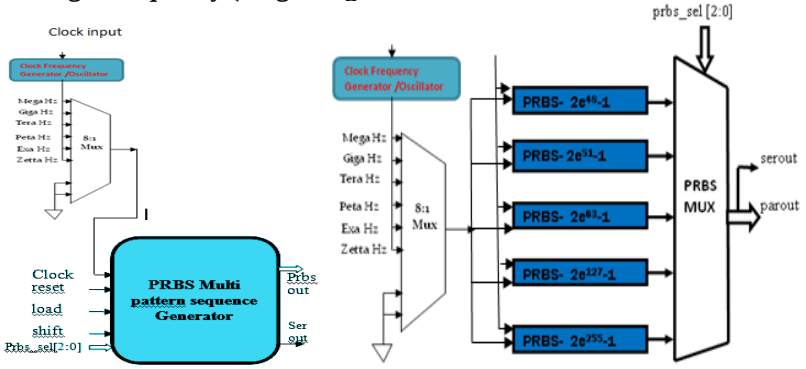


Figure 9: Ultra high frequency PRBS Model- Mega, Giga, Tera, Peta, Exa, Zetta HZ

Description: The above shows RTL Design Architecture of Ultra High Clock Frequency (Mega, Giga, Tera, Peta, Exa ,Zetta Hertz Clock) synchronized PRBS Multi pattern sequence generator Of $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 Tapped sequence patterns. It consists clock ,reset, load, shift, prbs sel, prbs parallel out and serial out signals. **The tapping elements are** (46,47), (48,51),(58,63), (122,127),(247,255) are compared(XOR)

bit by bit with each other generate Long periodic seed word carrier wave bit patterns based on the specific periodic length.

[C1] Proposed Tera Hertz PRBS Architectures

Tera Hz Clock PRBS Designs $2e^{48}$-1,$2e^{51}$-1, $2e^{63}$-1,$2e^{127}$-1, $2e^{255}$-1

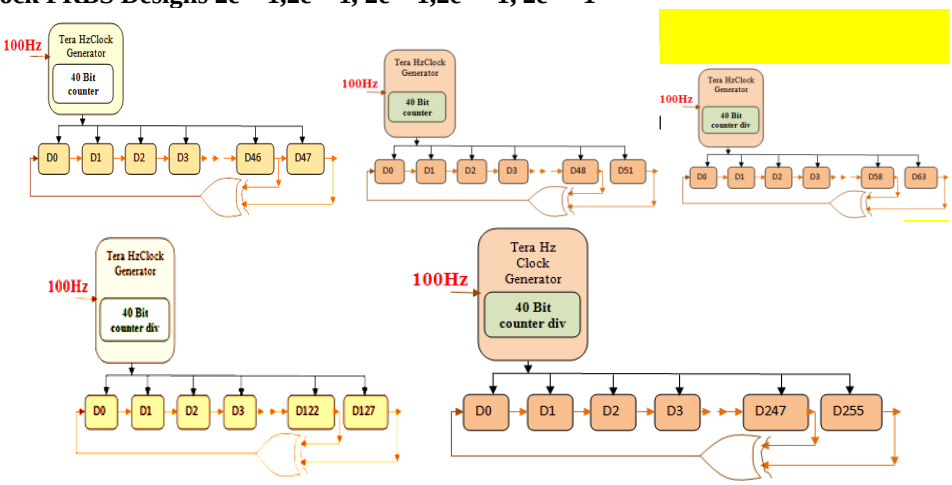


Figure 10: Tera Hertz Clock PRBS2e48-1,2e51-1, 2e63-1,2e127-1,2e255-1

Description: The Above Figure Designs describe Tera Herz Clock operated $2e^{48}$-1,$2e^{51}$-1, $2e^{63}$-1,$2e^{127}$-1,$2e^{255}$-1 PRBS tapped patterns with tapping elements (46,47), (48,51),(58,63), (122,127),(247,255) are compared(XOR) bit by bit with each other generate Long periodic seed word carrier wave bit patterns based on the specific periodic length. The transmission and reception done in the form of (6X8bit),(12X8bit) etc and these carriers can easily protect very low frequency base band signal for Ultra High long distance wireless communication Satellite / Space level Distance in terms of multiple lacks of distance KM's with out loss of signal.

Zetta Hz Clock PRBS Designs $2e^{48}$-1,$2e^{51}$-1, $2e^{63}$-1,$2e^{127}$-1, $2e^{255}$-1

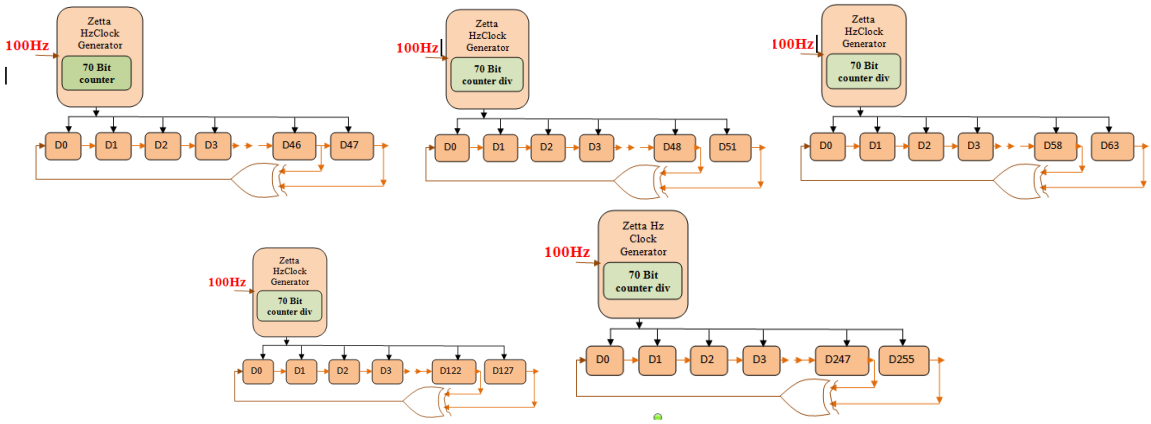


Figure 11: Zetta Hertz Clock PRBS2e48-1,2e51-1, 2e63-1,2e127-1,2e255-1

Description: The Above Designs describe Zetta Herz Clock operated $2e^{48}$-1,$2e^{51}$-1, $2e^{63}$-1,$2e^{127}$-1,$2e^{255}$-1 PRBS tapped patterns with tapping elements (46,47), (48,51),(58,63), (122,127),(247,255) are compared(XOR) bit by bit with each other generate Long periodic seed word carrier wave bit patterns based on the specific periodic length. The transmission and reception done in the form of (6X8bit),(12X8bit) etc and these carriers can easily protect very low frequency base band signal for Ultra High long distance wireless communication Satellite / Space level Distance in terms of multiple lacks of distance KM's with out loss of signal. This is future 7^{th} sense Design for smart computing designs.

III. Conclusion

*The RTL Design and Verification of PRBS Generator designed using long Periodicity PRBS Pattern Seed words-**are** $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$- 1, $2e^{255}$-1 for ultra high long distance space/satellite distance*

applications/products. The Aim of design forgenerate effective high frequency modulation and demodulation for long distance wireless communication applications as well improvement of system Bandwidth.

References

[1] "Itu-T Recommendation O.150". October 1992.
[2] Tomlinson, Kurt (4 February 2015). "Prbs (Pseudo-RandomBinary Sequence)". Bloopist. Retrieved 21 January 2016.
[3] Paul H. Bardell, William H. Mcanney, And Jacob Savir, "Built-In Test For Vlsi: Pseudorandom Techniques", John Wiley& Sons, New York, 1987.
[4] Wikipedia, "Http://En.Wikipedia.Org/Wiki/ Pseudorandom_Binary_Sequence"
[5] Wikipedia "Http://En.Wikipedia.Org/Wiki/ Linear_Feedback_Shift_Register"
[6] Sy Hwang, Gy Park, Dh Kim, Ks Jhang, "Efficient Implementation Of A Pseudorandom Sequence Generator For High-Speed Data Communications", Etri Journal, Volume 32, Number2, April 2010.
[7] Itu – Ccitt Reference Document [1] A Chow, Ws Coats, DHopkins, "A Configurable Asynchronous Pseudorandom Bit Sequence Generator", 13th Ieee International Symposium On Asynchronous Circuits And Systems (Async 07), Page(S): 143 - 152, March 2007.
[8] Xilinx Data Sheet Xapp884 (V1.0) January 10, 2011[9]. 1730ahmad, A., Nanda, N. K., And Garg, K., Mac
[9] Williams, Fj 1976, Pseudo Random Sequences & Arrays ,Ieee Proc., 1715- "An Efficient Design Of Maximal Length Of Pseudorandom Test Pattern Generators," Proceedings Of Ieee International Conference On Signals & Systems
[10] Riccardi, Daniele; Novellini, Paolo (10 January 2011). "An Attribute-Programmable Prbs Generator And Checker (Xap884)"(Pdf). Xilinx. Table 3:Configuration For Prbs Polynomials Most Used To Test Serial Lines. Retrieved 21 January 2016.
[11] "O.150 : General Requirements For Instrumentation For Performance Measurements On Digital Transmission Equipment"
[12] Https://Www.Intel.Com/Content/Www/Us/En/Docs/Programmable/683621/Current/Prbs-Pattern-Generator.Html
[13] Paul H. Bardell, William H. Mcanney, And Jacob Savir, "Built-In Test For Vlsi: Pseudorandom Techniques", John Wiley& Sons, New York, 1987.
[14] Sy Hwang, Gy Park, Dh Kim, Ks Jhang, "Efficient Implementation Of A Pseudorandom Sequence Generator For High-Speed Data Communications", Etri Journal, Volume 32, Number2, April 2010.